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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/006,559	12/03/2001	Antony Davies	01-52	2651

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LATTICE SEMICONDUCTOR CORPORATION
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EXAMINER	
GHULAMALI, QUTBUDDIN	

ART UNIT	PAPER NUMBER
2637	

DATE MAILED: 08/23/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/006,559	DAVIES ET AL.	
	Examiner	Art Unit	
	Qutub Ghulamali	2637	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,5,7,8,11,12,14,15,19 and 21-30* is/are rejected.

7)☒ Claim(s) *2-4, 6,9,10,13,16-8, 20* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This Office Action is responsive to the Amendment filed on 06/08/2005.

2. The objection to the specification cited in the Office Action of 03/09/2005 is withdrawn in view of the amendment to the Abstract of the Disclosure submitted by the applicant dated 06/08/2005. The amended abstract is acceptable.

Response to Arguments

3. Applicant's arguments/remarks filed 06/08/2005 with reference to anticipated rejection of claims 22 under 35 USC 102(b) to Anderson, has been fully considered but is not persuasive. The applicant argues, regarding "the multiplexer first selects a pair of given clock signals and the phase interpolator then interpolates between them, requires that only one phase interpolation be done". The examiner however, would respectfully like to draw applicant's attention to the claimed subject matter which recites that the multiplexer receives a plurality of clock signals having different phases to select each of at least two clock signals to generate a recovered clock signal whose phase is interpolated between phases of the at least two clocks. Anderson with reference to figs. 2, 3, (col. 2, lines 56-67; col. 3, lines 1-8), very clearly reads on the claimed subject matter highlighted above. Anderson further discloses that his interpolator achieves clock recovery without being limited to speed of the technology or by the number of delay elements used through use of the phase interpolator thereby reducing power consumption of the VCO.

A similar explanation applies with reference to claims 1, 8, 15, and 27-29, that Anderson does in fact meet the requirements of the claimed limitations.

For this reason and the reasons stated in the previous office action mailed 3/09/05 and reiterated herein, the rejections of the claims are maintained.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1, 5, 15, 19, 22, 27-30 are rejected under 35 U.S.C. 102(b) as being anticipated by Anderson (US Patent 6,122,336).

Regarding claims 1 and 15, Anderson discloses a Digital clock recovery circuit for generating a recovered clock signal, the phase selector comprising:

a phase select signal generator (abstract; figs. 1, 2, element 102, 208) for generating a plurality of phase select signals in response to a FWD signal and a BWD signal from a digital filter (106, 204) (abstract; col. 1, lines 20-25);

wherein said digital filter (204) asserts said FWD signal (216) if the phase of a SDIN (serial digital input) signal leads the phase of said recovered clock signal (col. 3, lines 11-20);

and wherein said digital filter asserts said BWD signal (218) if the phase of said SDIN (serial digital input) signal lags the phase of said recovered clock signal (col. 3, lines 11-20);

a multiplexer (synthesizer 208) for inputting a predetermined number of given clock signals arranged in a predetermined phase order and for outputting a first output clock signal and a second output clock signal with said first and second output clock signals each being one of said given clock signals (col. 2, lines 56-67, col. 3, lines 1-8);

a phase interpolator (210) that receives said first and second output clock signals from said multiplexer to generate said recovered clock signal having a phase that is phase interpolated between the phases of said first and second output clock signals (col. 2, lines 56-67; col. 3, lines 1-8); and

a multiplexer select control that controls said multiplexer to select one of said given clock signals for each of said first and second output clock signals, depending on whether said phase select signals indicate that said FWD signal is asserted or that said BWD signal is asserted such that the phase of said recovered clock signal generated from said phase interpolator increases when said FWD signal is asserted and decreases when said BWD signal is asserted and remains substantially constant when said FWD signal and said BWD signal are not asserted (col. 3, lines 19-30; col. 4, lines 49-55).

Regarding claims 5 and 11, Anderson discloses a predetermined number of given clock signals is sent to said multiplexer from a voltage controlled oscillator (frequency synthesizer 800 includes a VCO) with any two adjacent given clock signals (ring oscillator) in said predetermined phase order of said given clock signals having a substantially same phase difference and with first and last given clock signals in said predetermined phase order of said given clock signals having said substantially same phase difference (col 1, lines 11-25).

Regarding claim 19, Anderson discloses any two adjacent given clock signals (ring oscillator) in said predetermined phase order of said given clock signals having a substantially same phase difference (45 degrees) and with first and last given clock signals in said predetermined phase order of said given clock signals having said substantially same phase difference (col. 4, lines 12-27).

Regarding claim 22 and 28, Anderson discloses a Digital clock recovery circuit for generating a recovered clock signal comprising:

a phase detector (fig. 2, element 202) operable to compare a serial data input (SDIN) with a recovered clock signal (SCLK) and to generate in response up and down signals (col. 3, lines 9-13);

a digital filter (204) coupled between the phase detector (202) and operable to generate forward and backward signals in response to the up and down signals (212, 214) (col. 3 lines 15-30); and a phase selector (206) coupled to the digital filter (204) and including a phase interpolator (210) coupled to a multiplexer (synthesizer 208) responsive to the forward and backward signals, the multiplexer (synthesizer) operable to receive a plurality of given clock signals having different phases as inputs and to select each of at least two clock signals as one of the given clock signals as outputs, the phase interpolator operable to generate a recovered clock signal having a phase that is phase interpolated between the phases of the at least two selected clock signals (col. 2, lines 56-67; col. 3, lines 1-8).

Regarding claim 27, Anderson discloses a phase selector comprising:

a phase select signal generator responsive to forward and backward signals and operable to generate a multiplexer select signal (col. 5, lines 15-28);

a multiplexer (synthesizer 208) coupled to the phase select signal generator and operable to receive a plurality of given clock signals having different phases as inputs and to select each of at least two of the clock signals as one of the given clock signals as outputs (col. 5, lines 28-33); and

a phase interpolator (210) coupled to the multiplexer and operable to generate a recovered clock signal (SCLK) having a phase that is phase interpolated between the phases of the at least two selected clock signals (col. 2, lines 56-67; col. 3, lines 1-8).

As per claim 29, Anderson discloses generating a recovered clock signal comprise:

providing a plurality of given clock signals (abstract; 2N clocks) having different phases (fig. 4; col. 3, lines 66-67; col. 4, lines 1-2);

select each of at least two clock signals as one of the given clock signals as outputs, in response to received forward and backward signals; and

generating a recovered clock signal (SCLK) having a phase that is phase interpolated between the phases of the at least two selected clock signals (col. 2, lines 56-67; col. 3, lines 1-8).

Regarding claim 30, Anderson discloses, the multiplexer is operable to select the same clock signal as the at least two selected clock signals (col. 5, lines 30-41).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 7, 8, 11, 12, 14, 21, 23-26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Anderson (US Patent 6,122,336) in view of Aung et al (US Pub. 2003/0212930).

Regarding claims 7, 14, 21 and 23, Anderson discloses substantially every feature of the claimed invention above. Anderson however, is silent regarding part of the data recovery circuit within a serializer/deserializer transceiver. Aung, in the same field of endeavor, discloses the DPLL is part of a data recovery circuit within a serializer/deserializer transceiver (fig. 10, elements 340b, 60b). It would have been obvious to a person skilled in the art at the time the invention was made to use the DPLL within a serializer/deserializer circuit as taught by Aung in the clock recovery circuit of Anderson because it can support a wide range of clock data recovery signaling protocols in a very flexible manner.

With reference to claim 8, steps claimed as means is nothing more than restating the function of the specific components of the apparatus as claimed above and therefore, it would have been obvious, considering the aforementioned rejection for the apparatus claim 1.

Regarding claim 11, Anderson discloses said predetermined order of said phase select signals is a closed loop with a first phase select signal being adjacent a last phase select signal in said closed loop of said predetermined order of said phase select signals (col. 1, lines 11-25).

Regarding claim 12, Anderson discloses any two adjacent given clock signals (ring oscillator) in said predetermined phase order of said given clock signals having a substantially same phase difference (45 degrees) and with first and last given clock signals in said predetermined phase order of said given clock signals having said substantially same phase difference (col. 4, lines 12-27).

As per claim 24, Anderson discloses the phase selector includes a phase select signal generator coupled to the multiplexer, the generator responsive to the forward and backward signals and operable to generate a multiplexer select signal (col. 5, lines 15-28).

As per claim 25, Anderson discloses, the phase select generator comprises (fig. 10) a plurality of bi-directional flip-flops with each flip-flop having an output signal that is a multiplexer select signal (col. 5, lines 28-41).

Regarding claim 26, Anderson discloses, the multiplexer is operable to select the same clock signal as the at least two selected clock signals (col. 5, lines 30-41).

Allowable Subject Matter

5. Claims 2-4, 6, 9, 10, 13, 16-18, 20 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent and to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action form including all of the limitations of the base claim and any intervening claims.

Conclusion

6. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period

will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Qutub Ghulamali whose telephone number is (571) 272-3014. The examiner can normally be reached on Monday-Friday from 8:00AM - 5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jay Patel can be reached on (571) 272-2988. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

QG.
August 19, 2005.

JAY K. PATEL
SUPERVISORY PATENT EXAMINER